

## FDB045AN08A0

### N-Channel PowerTrench® MOSFET

75 V, 80 A, 4.5 mΩ

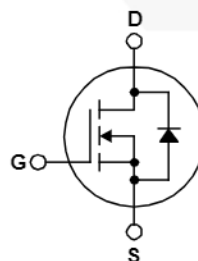
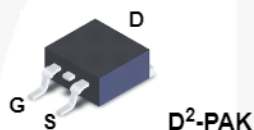
#### Features

- $R_{DS(on)} = 3.9\text{ m}\Omega$  (Typ.) @  $V_{GS} = 10\text{ V}$ ,  $I_D = 80\text{ A}$
- $Q_{G(tot)} = 92\text{ nC}$  (Typ.) @  $V_{GS} = 10\text{ V}$
- Low Miller Charge
- Low  $Q_{rr}$  Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

#### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies

Formerly developmental type 82684



#### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDB045AN08A0	Units
$V_{DSS}$	Drain to Source Voltage	75	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_C < 137^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	90	A
	Continuous ( $T_{amb} = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ , with $R_{\theta JA} = 43^\circ\text{C/W}$ )	19	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	600	mJ
$P_D$	Power dissipation	310	W
	Derate above $25^\circ\text{C}$	2.0	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	0.48	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, 1in <sup>2</sup> copper pad area	43	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB045AN08A0	FDB045AN08A0	D <sup>2</sup> -PAK	330 mm	24 mm	800 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	75	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 80\text{A}, V_{GS} = 10\text{V}$	-	0.0039	0.0045	$\Omega$
		$I_D = 37\text{A}, V_{GS} = 6\text{V}$	-	0.0056	0.0084	
		$I_D = 80\text{A}, V_{GS} = 10\text{V},$ $T_J = 175^\circ\text{C}$	-	0.008	0.011	

### Dynamic Characteristics

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	6600	-	pF
$C_{OSS}$	Output Capacitance		-	1000	-	pF
$C_{RSS}$	Reverse Transfer Capacitance		-	240	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}$	-	92	138	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V to } 2\text{V}$	-	11	17	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 40\text{V}$ $I_D = 80\text{A}$ $I_g = 1.0\text{mA}$	-	27	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	16	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	21	-	nC

### Switching Characteristics ( $V_{GS} = 10\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 40\text{V}, I_D = 80\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 3.3\Omega$	-	-	160	ns
$t_{d(ON)}$	Turn-On Delay Time		-	18	-	ns
$t_r$	Rise Time		-	88	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	40	-	ns
$t_f$	Fall Time		-	45	-	ns
$t_{OFF}$	Turn-Off Time		-	-	128	ns

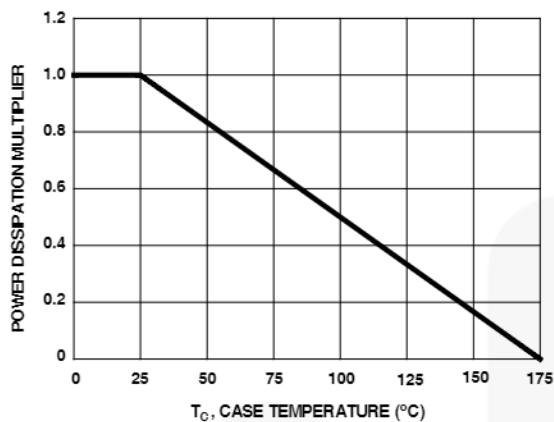
### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}$	-	-	1.25	V
		$I_{SD} = 40\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 75\text{A}, di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	53	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 75\text{A}, di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	54	nC

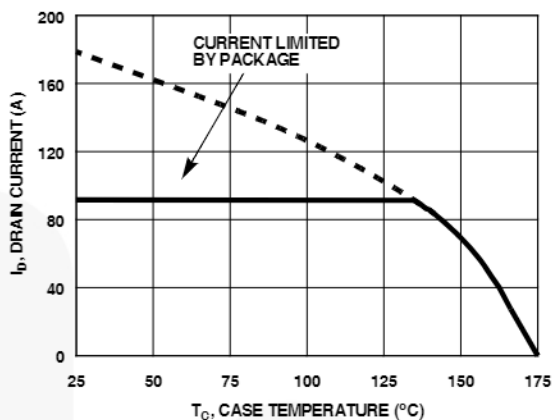
#### Notes:

- 1: Starting  $T_J = 25^\circ\text{C}, L = 0.48\text{mH}, I_{AS} = 50\text{A}$ .
- 2: Pulse Width = 100s

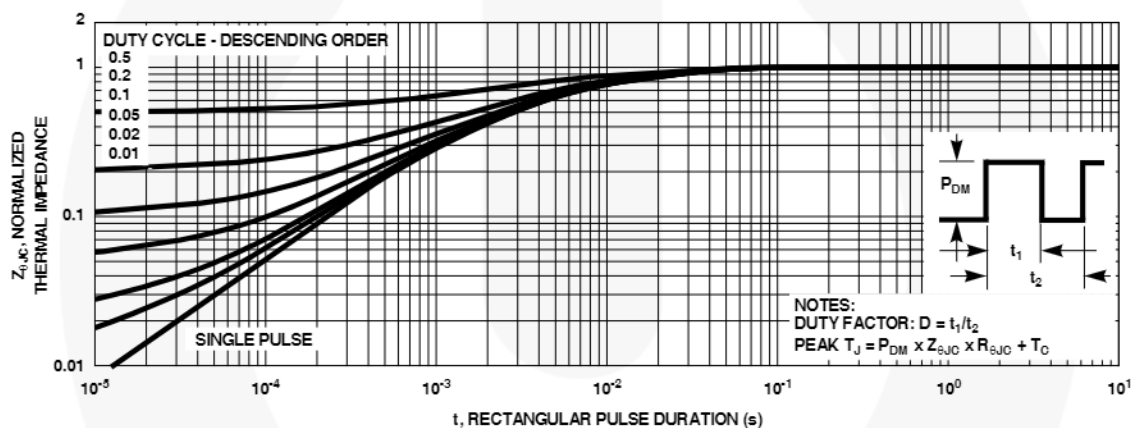
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



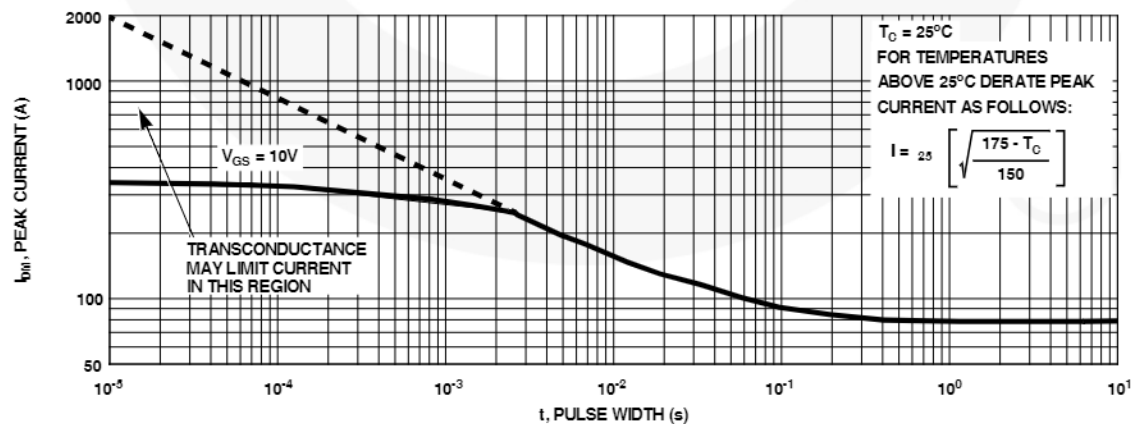
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**



**Figure 3. Normalized Maximum Transient Thermal Impedance**



**Figure 4. Peak Current Capability**

**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

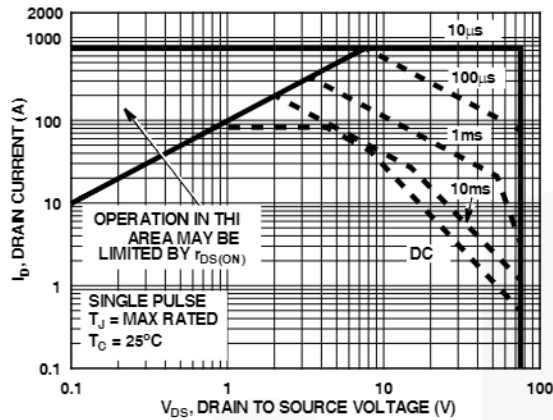
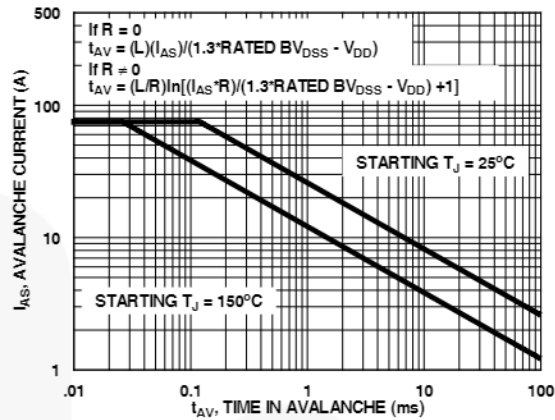


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515  
**Figure 6. Unclamped Inductive Switching Capability**

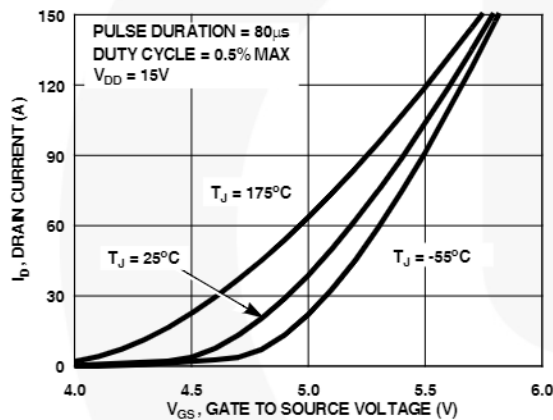


Figure 7. Transfer Characteristics

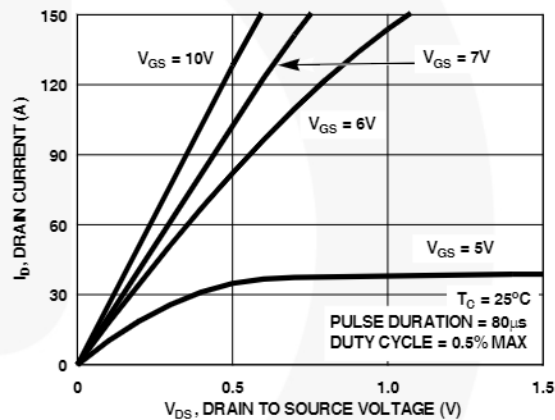


Figure 8. Saturation Characteristics

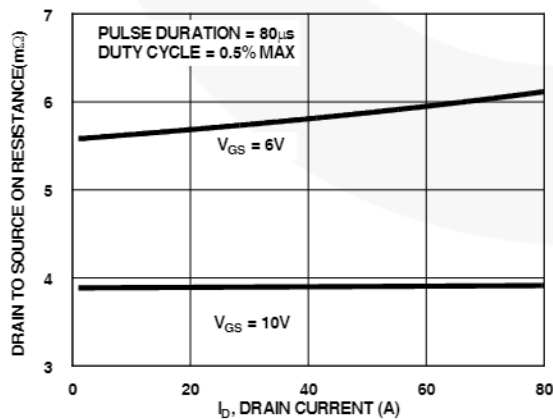


Figure 9. Drain to Source On Resistance vs Drain Current

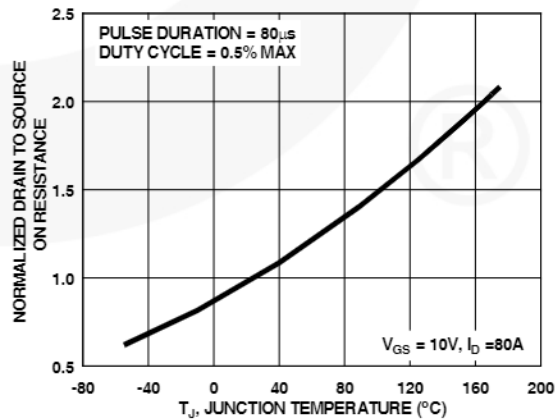
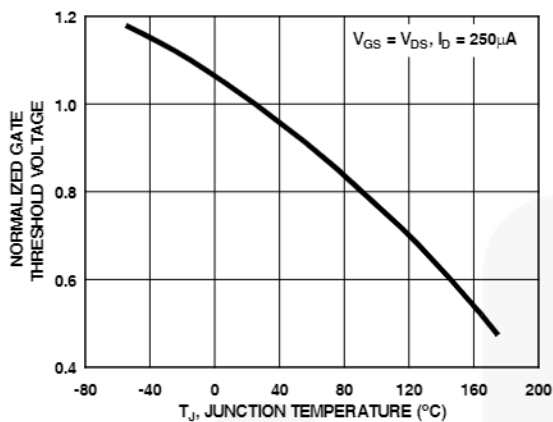
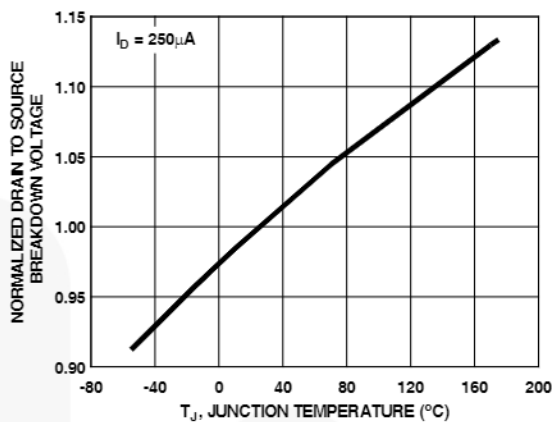


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

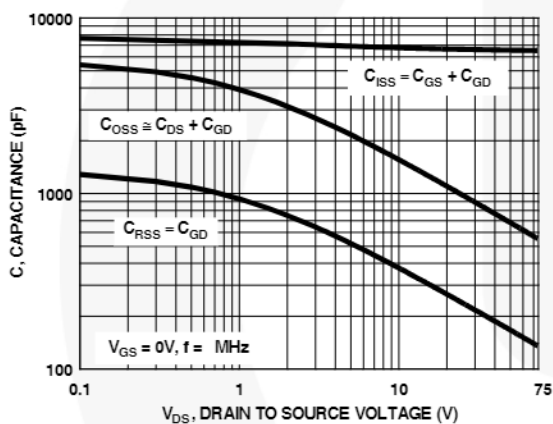
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



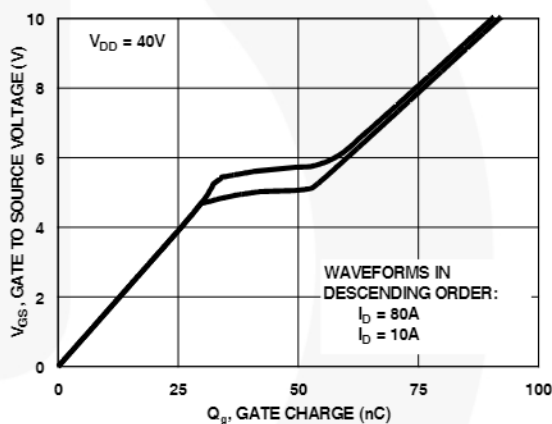
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Currents**

## Test Circuits and Waveforms

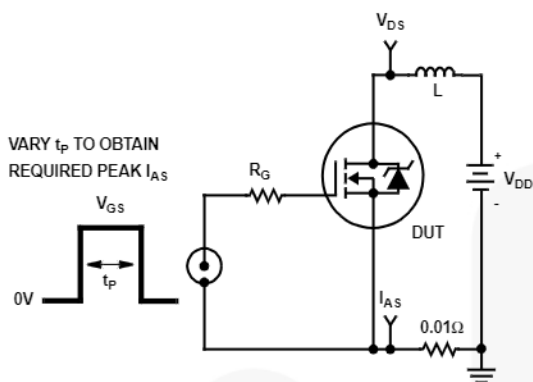


Figure 15. Unclamped Energy Test Circuit

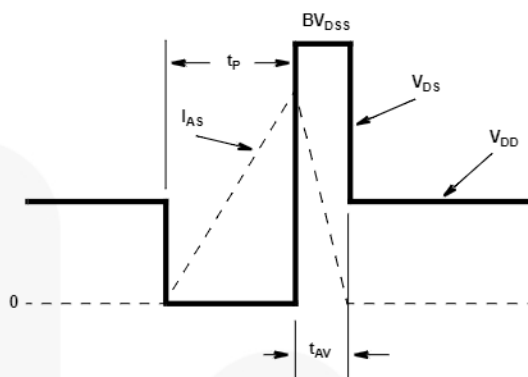


Figure 16. Unclamped Energy Waveforms

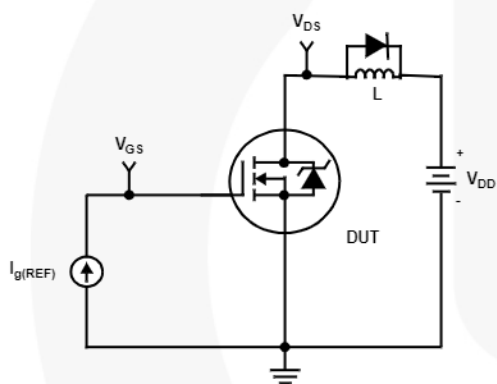


Figure 17. Gate Charge Test Circuit

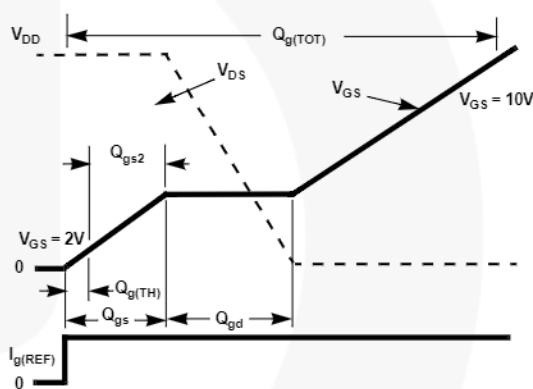


Figure 18. Gate Charge Waveforms

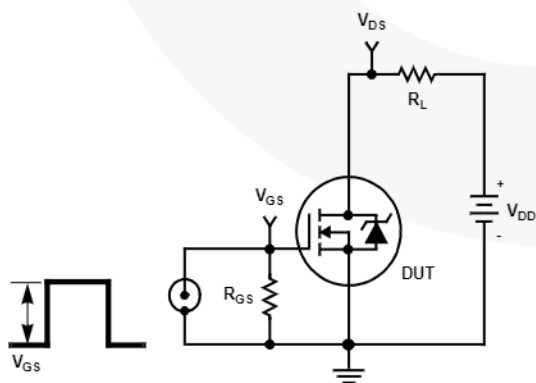


Figure 19. Switching Time Test Circuit

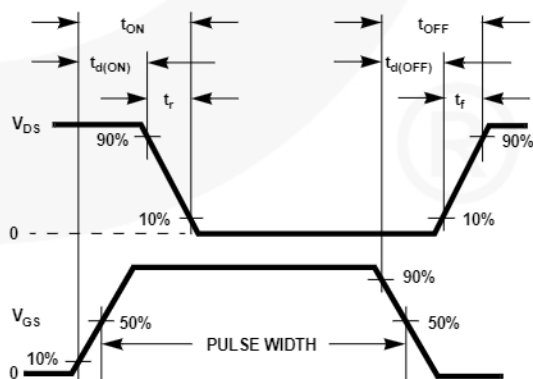


Figure 20. Switching Time Waveforms

### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  ( $^{\circ}C$ ), and thermal resistance  $R_{\theta JA}$  ( $^{\circ}C/W$ ) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $P_{DM}$  is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \quad (\text{EQ. 2})$$

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)} \quad (\text{EQ. 3})$$

Area in Centimeters Squared

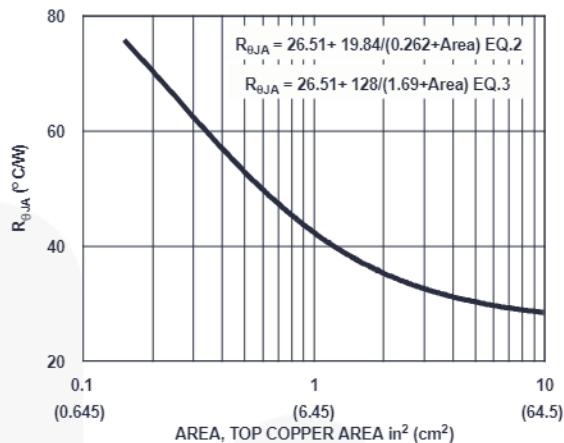


Figure 21. Thermal Resistance vs Mounting Pad Area

### PSPICE Electrical Model

.SUBCKT FDB045AN08A0 2 1 3 ; rev March 2002  
 CA 12 8 1.5e-9  
 CB 15 14 1.5e-9  
 CIN 6 8 6.4e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 82.3  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 4.81e-9  
 LSOURCE 3 7 4.63e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 9e-4  
 RGATE 9 20 1.36  
 RLDRAIN 2 5 10  
 RLGATE 1 9 48.1  
 RLSOURCE 3 7 46.3  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 2.3e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE=((V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51))/(1e-6\*250),10))

.MODEL DBODYMOD D (IS = 2.4e-11 N = 1.04 RS = 1.76e-3 TRS1 = 2.7e-3 TRS2 = 2e-7 XTI=3.9 CJO = 4.35e-9 TT = 1e-8 M = 5.4e-1)

.MODEL DBREAKMOD D (RS = 1.5e-1 TRS1 = 1e-3 TRS2 = -8.9e-6)

.MODEL DPLCAPMOD D (CJO = 1.35e-9 IS = 1e-30 N = 10 M = 0.53)

.MODEL MMEDMOD NMOS (VTO = 3.7 KP = 9 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.36)

.MODEL MSTROMOD NMOS (VTO = 4.4 KP = 250 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)

.MODEL MWEAKMOD NMOS (VTO = 3.05 KP = 0.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.36e1 RS = 0.1)

.MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = -9e-7)

.MODEL RDRAINMOD RES (TC1 = 1.9e-2 TC2 = 4e-5)

.MODEL RSLCMOD RES (TC1 = 1.3e-3 TC2 = 1e-5)

.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)

.MODEL RVTHRESMOD RES (TC1 = -6e-3 TC2 = -1.9e-5)

.MODEL RVTEMPMOD RES (TC1 = -2.4e-3 TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.0 VOFF = -1.5)

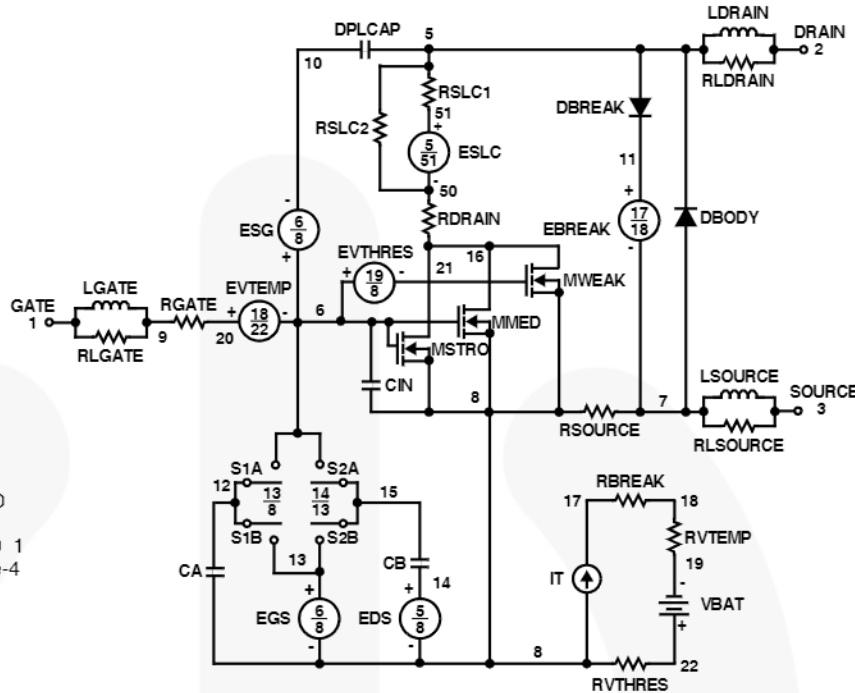
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF = -4.0)

.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.0 VOFF = 0.5)

.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.0)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.







### SPICE Thermal Model

REV 23 March 2002

FDB045AN08A0T

CTHERM1 th 6 6.45e-3  
 CHERM2 6 5 3e-2  
 CHERM3 5 4 1.4e-2  
 CHERM4 4 3 1.65e-2  
 CHERM5 3 2 4.85e-2  
 CHERM6 2 tl 1e-1

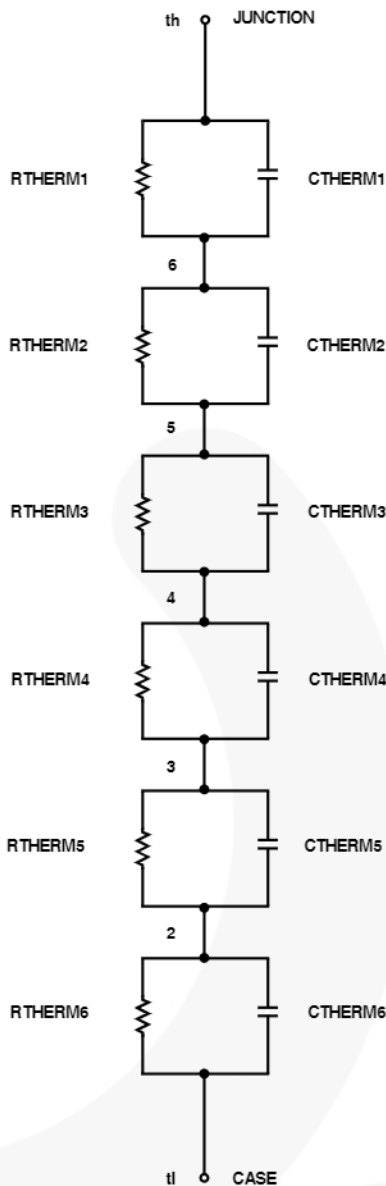
RHERM1 th 6 3.24e-3  
 RHERM2 6 5 8.08e-3  
 RHERM3 5 4 2.28e-2  
 RHERM4 4 3 1e-1  
 RHERM5 3 2 1.1e-1  
 RHERM6 2 tl 1.4e-1

### SABER Thermal Model

SABER thermal\_model FDB045AN08A0T  
 template thermal\_model th tl  
 thermal\_c th, tl

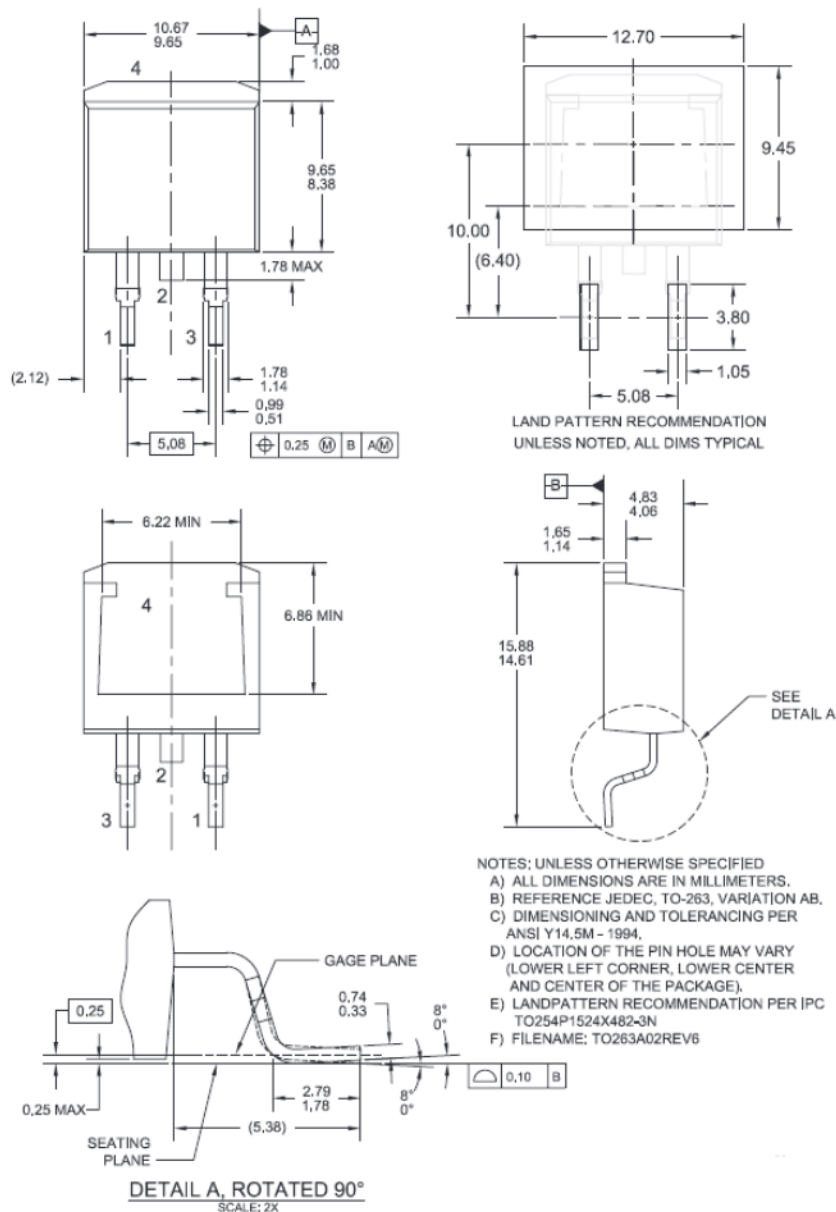
```
{
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    ctherm.ctherm2 6 5 = 3e-2
    ctherm.ctherm3 5 4 = 1.4e-2
    ctherm.ctherm4 4 3 = 1.65e-2
    ctherm.ctherm5 3 2 = 4.85e-2
    ctherm.ctherm6 2 tl = 1e-1
```

```
rtherm.rtherm1 th 6 = 3.24e-3
rtherm.rtherm2 6 5 = 8.08e-3
rtherm.rtherm3 5 4 = 2.28e-2
rtherm.rtherm4 4 3 = 1e-1
rtherm.rtherm5 3 2 = 1.1e-1
rtherm.rtherm6 2 tl = 1.4e-1
}
```



## Mechanical Dimensions

### TO-263 2L (D<sup>2</sup>PAK)



**Figure 22. 2LD, TO263, Surface Mount**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:




[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TT263-002](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT263-002)

Dimension in Millimeters



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| AX-CAP®*   | FRFET®  | PowerXS™  | <b>S SYSTEM GENERAL</b> ®*  |
| BitSiC™  | Global Power ResourceSM                         | Programmable Active Droop™  | TinyBoost®  |
| Build it Now™  | GreenBridge™                                    | QFET®   | TinyBuck®   |
| CorePLUS™  | Green FPS™                                      | QS™   | TinyCalc™   |
| CorePOWER™   | Green FPS™ e-Series™                            | Quiet Series™   | TinyLogic®  |
| CROSSVOLT™   | Gmax™   | RapidConfigure™   | TINYOPTO™   |
| CTL™   | GTO™  |   | TinyPower™  |
| Current Transfer Logic™  | IntelliMAX™                                     |  Saving our world, 1mW/W/kW at a time™ | TinyPWM™  |
| DEUXPEED®  | ISOPLANAR™                                      | SignalWise™   | TinyWire™   |
| Dual Cool™   | Marking Small Speakers Sound Louder and Better™ | SmartMax™   | TranSiC™  |
| EcoSPARK®  | MegaBuck™                                       | SMART START™  | TriFault Detect™  |
| EfficientMax™  | MICROCOUPLER™                                   | Solutions for Your Success™   | TRUECURRENT®*   |
| ESBC™  | MicroFET™                                       | SPM®  | µSerDes™  |
|  Fairchild® | MicroPak™                                       | STEALTH™  |  SerDes® |
| Fairchild Semiconductor®   | MicroPak2™                                      | SuperFET®   | UHC®  |
| FACT Quiet Series™   | MillerDrive™                                    | SuperSOT™-3   | Ultra FRFET™  |
| FACT®  | MotionMax™                                      | SuperSOT™-6   | UniFET™   |
| FAST®  | mWSaver®  | SuperSOT™-8   | VCX™  |
| FastvCore™   | OptoHiT™  | SupreMOS®   | VisualMax™  |
| FETBench™  | OPTOLOGIC®                                      | SyncFET™  | VoltagePlus™  |
| FPS™   | OPTOPLANAR®                                     |   | XS™   |

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- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support. Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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